differential output coupled to a signal processing circuitry having an input impedance,

wherein the impedance matching network matches the input impedance of the signal processing circuitry to the output impedance of the filter circuitry.

3. The front-end circuitry according to claim 1, wherein the filter circuitry receives a radio-frequency input signal.

4. The front-end circuitry according to claim 3, wherein the signal processing circuitry comprises an amplifier circuitry.

5. The front-end circuitry according to claim 4, wherein signal processing circuitry comprises a low-noise amplifier circuitry.

6. The front-end circuitry according to claim 5, wherein the impedance matching network comprises a differential L-network.

7. The front-end circuitry according to claim 6, wherein the signal processing circuitry comprises a single-ended output.

8. The front-end circuitry according to claim 6, wherein the signal processing circuitry comprises a differential output.

9. The front-end circuitry according to claim 6, wherein the differential L-network comprises two inductors and a capacitor.

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10. The front-end circuitry according to claim 6, wherein the differential L-network comprises two capacitors and an inductor.

11. The front-end circuitry according to claim 5, wherein the impedance matching network comprises a plurality of differential L-networks.

12. The front-end circuitry according to claim 11, wherein the signal processing circuitry comprises a single-ended output.

13. The front-end circuitry according to claim 11, wherein the signal processing circuitry comprises a differential output.

14. The front-end circuitry according to claim 5, wherein the impedance matching network comprises a differential Π-network.

15. The front-end circuitry according to claim 14, wherein the signal processing circuitry comprises a single-ended output.

16. The front-end circuitry according to claim 14, wherein the signal processing circuitry comprises a differential output.

17. The front-end circuitry according to claim 14, wherein the differential Π-network comprises two inductors and two capacitors.

18. The front-end circuitry according to claim 5, wherein the impedance matching network comprises a plurality of differential Π-networks.

19. The front-end circuitry according to claim 18, wherein the signal processing circuitry comprises a single-ended output.

20. The front-end circuitry according to claim 18, wherein the signal processing circuitry comprises a differential output.

21. The front-end circuitry according to claim 5, wherein the impedance matching network comprises a differential T-network.

22. The front-end circuitry according to claim 21, wherein the signal processing circuitry comprises a single-ended output.

23. The front-end circuitry according to claim 21, wherein the signal processing circuitry comprises a differential output.

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24. The front-end circuitry according to claim 21, wherein the differential T-network comprises four inductors and one capacitor.

25. The front-end circuitry according to claim 21, wherein the differential T-network comprises four capacitors and one inductor.

26. The front-end circuitry according to claim 5, wherein the impedance matching network comprises a plurality of differential T-networks.

27. The front-end circuitry according to claim 26, wherein the signal processing circuitry comprises a single-ended output.

28. The front-end circuitry according to claim 26, wherein the signal processing circuitry comprises a differential output.

29. The front-end circuitry according to claim 5, wherein the impedance matching network comprises at least one of a differential L-network, a differential Π-network, a differential T-network, or a combination thereof coupled in cascade.

30. The front-end circuitry according to claim 29, wherein the signal processing circuitry comprises a single-ended output.

31. The front-end circuitry according to claim 29, wherein the signal processing circuitry comprises a differential output.

32. The front-end circuitry according to claim 5, wherein the impedance matching network comprises a differential transmission line.

33. The front-end circuitry according to claim 32, wherein the signal processing circuitry comprises a single-ended output.

34. The front-end circuitry according to claim 32, wherein the signal processing circuitry comprises a differential output.

35. A radio-frequency (RF) apparatus, comprising:

an impedance matching network, having a differential input and a differential output; and

a filter configured to receive a radio-frequency input signal, the filter having a differential output configured to provide a filtered signal to the impedance matching network.

36. The radio-frequency apparatus of claim 35, further comprising a signal-processing circuit having a differential input, the signal-processing circuit configured to accept a signal from the differential output of the impedance matching network.

37. The radio-frequency apparatus of claim 36, wherein the impedance matching network matches an output impedance of the filter to an input impedance of the signal-processing circuit.

38. The radio-frequency apparatus of claim 37, wherein the impedance matching network comprises at least one differential L-network.

39. The radio-frequency apparatus of claim 38, wherein the signal-processing circuit comprises a low-noise amplifier.

40. The radio-frequency apparatus of claim 39, further comprising a first integrated circuit, wherein the low-noise amplifier resides within the first integrated circuit.

41. The radio-frequency apparatus of claim 40, wherein the first integrated circuit further comprises radio-frequency receiver circuitry.

42. The radio-frequency apparatus of claim 41, further comprising a second integrated comprising digital signal-processing circuitry, the second integrated circuit coupled to the first integrated circuit and configured to accept a digital output signal of the first integrated circuit.

43. The radio-frequency apparatus of claim 37, wherein the impedance matching network comprises at least one differential Π-network.

44. The radio-frequency apparatus of claim 43, wherein the signal-processing circuit comprises a low-noise amplifier.

45. The radio-frequency apparatus of claim 44, further comprising a first integrated circuit, wherein the low-noise amplifier resides within the first integrated circuit.

46. The radio-frequency apparatus of claim 45, wherein the first integrated circuit further comprises radio-frequency receiver circuitry.

47. The radio-frequency apparatus of claim 46, further comprising a second integrated comprising digital signal-processing circuitry, the second integrated circuit coupled to the first integrated circuit and configured to accept a digital output signal of the first integrated circuit.

48. The radio-frequency apparatus of claim 37, wherein the impedance matching network comprises at least one differential T-network.

49. The radio-frequency apparatus of claim 48, wherein the signal-processing circuit comprises a low-noise amplifier.

50. The radio-frequency apparatus of claim 49, further comprising a first integrated circuit, wherein the low-noise amplifier resides within the first integrated circuit.

51. The radio-frequency apparatus of claim 50, wherein the first integrated circuit further comprises radio-frequency receiver circuitry.

52. The radio-frequency apparatus of claim 51, further comprising a second integrated comprising digital signal-processing circuitry, the second integrated circuit coupled to the first integrated circuit and configured to accept a digital output signal of the first integrated circuit.

53. The radio-frequency apparatus of claim 37, wherein the impedance matching network comprises a cascade coupling of at least one differential L-network, at least one differential Π-network, at least one differential T-network, or a combination thereof.

54. The radio-frequency apparatus of claim 53, wherein the signal-processing circuit comprises a low-noise amplifier.

55. The radio-frequency apparatus of claim 54, further comprising a first integrated circuit, wherein the low-noise amplifier resides within the first integrated circuit.

56. The radio-frequency apparatus of claim 55, wherein the first integrated circuit further comprises radio-frequency receiver circuitry.

57. The radio-frequency apparatus of claim 56, further comprising a second integrated comprising digital signal-processing circuitry, the second integrated circuit coupled to the

first integrated circuit and configured to accept a digital output signal of the first integrated circuit.

58. The radio-frequency apparatus of claim 37, wherein the impedance matching network comprises a differential transmission line.

59. The radio-frequency apparatus of claim 58, wherein the signal-processing circuit comprises a low-noise amplifier.

60. The radio-frequency apparatus of claim 59, further comprising a first integrated circuit, wherein the low-noise amplifier resides within the first integrated circuit.

61. The radio-frequency apparatus of claim 60, wherein the first integrated circuit further comprises radio-frequency receiver circuitry.

62. The radio-frequency apparatus of claim 61, further comprising a second integrated comprising digital signal-processing circuitry, the second integrated circuit coupled to the first integrated circuit and configured to accept a digital output signal of the first integrated circuit.

63. A method of processing signals in a radio-frequency (RF) apparatus, comprising:

filtering an input radio-frequency signal in a filter that has a differential output configured to provide a filtered signal; and

receiving and processing the filtered signal in an impedance matching network that has a differential input, the impedance matching network configured to generate an output signal at a differential output of the impedance matching network.

64. The method of claim 63, wherein the impedance matching network is configured to match an output impedance of the filter to an input impedance of the signal-processing circuit.

65. The method of claim 64, further comprising processing the output signal in a radio-frequency receiver circuitry.

66. The method of claim 65, wherein processing the output signal in a radio-frequency receiver circuitry comprises processing the output signal in a low-noise amplifier.

67. The method of claim 66, wherein the impedance matching network for receiving and processing the filtered signal comprises at least one differential L-network.

68. The method of claim 66, wherein the impedance matching network for receiving and processing the filtered signal comprises at least one differential Π-network.

69. The method of claim 66, wherein the impedance matching network for receiving and processing the filtered signal comprises at least one differential T-network.

70. The method of claim 66, wherein the impedance matching network for receiving and processing the filtered signal comprises a cascade coupling of at least one differential L-network, at least one differential P-network, at least one differential T-network, or a combination thereof.

71. The method of claim 66, wherein the impedance matching network for receiving and processing the filtered signal comprises a differential transmission line.

72. The method of claim 66, wherein the impedance matching network for receiving and processing the filtered signal comprises at least one of a differential L-network, a differential P-network, and a differential T-network.

73. The method of claim 72, wherein the low-noise amplifier for processing the output signal resides in a first integrated circuit that includes the radio-frequency receiver circuitry.

74. The method of claim 73, further comprising:

receiving in a second integrated circuit a digital output signal of the radio-frequency receiver circuitry; and

processing digitally the digital output signal of the radio-frequency receiver circuitry.

CONCLUSION

A check in the amount of $954.00 is enclosed for excess claims. Should any additional fees under 37 CFR 1.16-1.21 be required for any reason relating to the enclosed materials, the Commissioner is authorized to deduct such fees from Deposit Account No. 10-1205/SILA:107. The examiner is invited to contact the undersigned at the phone number indicated below with any questions or comments, or to otherwise facilitate expeditious and compact prosecution of the application.

Respectfully submitted,

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